Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 61208

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2014.

Sixth Semester

Electronics and Communication Engineering

EC 1354 — VLSI DESIGN

(Common to Electrical and Electronics Engineering)

(Regulation 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is the special feature of Twin-Tub process?
2. What is Depletion mode Device?
3. What are the factors to be considered for transistor scaling?
4. What are the static properties of complementary CMOS Gates?
5. What are the issues to be considered for circuit characterization and performance estimation?
6. Define Delay time.
7. Mention the levels at which testing in a chip can be done.
8. Design a set of CMOS gates to implement the sum function.
9. Define FSM.
10. What are gate primitives?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain SOI fabrication process of CMOS transistor. (10)

(ii) Derive the design equations for MOS devices. (6)

Or

(b) (i) Explain the operation of NMOS Enhancement transistor. (6)

(ii) Explain the second order effects with their equations. (10)

12. (a) Explain the complimentary CMOS inverter DC characteristics. (16)

Or

(b) (i) Explain the concept of static and dynamic CMOS design. (8)

(ii) Explain the construction and operation of transmission gates. (8)

13. (a) Explain in detail about the following :

(i) Resistance estimation. (8)

(ii) Inductance estimation. (8)

Or

(b) With neat diagram explain about various types of power dissipation in CMOS inverter. (16)

14. (a) Give the design procedure and draw the circuit diagram and layout for 8 bit carry look ahead adder. (16)

Or

(b) Explain the concept of clock distribution and power distribution. (16)

15. (a) Explain the following with an example :

(i) Tasks and functions (4)

(ii) Test bench for 4 : 1 multiplexer (4)

(iii) Difference between always and initial (4)

(iv) Blocking and non-blocking statements. (4)

Or

(b) (i) Design and develop a project in HDL to compare x5x4x3x2x1x0 with y5y4y3y2y1y0. Check the output by means of test bench. (10)

(ii) Give the different types of operators in Verilog HDL and explain any three. (6)

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